Experiment No. 2
Op-Amp Imperfections
ECE 311

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Date Performed:	February 11
Instructor:	Professor Saletta

1 Introduction

This lab will explore offset, frequency response, maximum peak output voltage, rise-time, and slew rate limiting.

2 Procedure

a. Build and measure offset Op-Amp offset voltages.

b. Build a offset removal circuit.

c. Build a slew rate test circuit, and verify its operation.

d. Show how slew rate limiting takes place.

e. Build circuit to verifiy calcuations.

f. Measure amplifier bandwidth for differing gains.

3 Equipment

- Oscilloscope
- Function generator
- $\mu A741$
- resistors and capacitors

4 Observations

This section is more clearly broken into corresponding steps in the procedure.

4.1 Voltage Offset

4.1.1 Preliminary

When the V_{in} of the Op-Amp is 0, all other measured voltages should be zero.

4.1.2 Lab Results

Resistor Values	V_+	V_-	V_{out}
$R_2 = 10M\Omega, R_1 = 1M\Omega, R = 10M\Omega \parallel 1M\Omega$	-13mV	-15.5mV	25mV
$R_2 = 10M\Omega, R_1 = 1M\Omega, R = 0$	0	0	.183V
$R_2 = 10k\Omega, R_1 = 1k\Omega, R = 10k\Omega \parallel 1k\Omega$	.015mV	.4mV	1.2mV
$R_2 = 10k\Omega, R_1 = 1k\Omega, R = 0$	0	1.6mV	9.5V

4.2 Slew Rate

4.2.1 Preliminary

The rise time is $10Vtimes$ .8 (10% to 90%) $\times \frac{\mu s}{.5v} = 16\mu s$. The slew rate is $/fracI_{sc}C_L = \frac{25ma}{100pF} = 250\frac{V}{\mu s}$, which is larger than the internal slew rate of $.5\frac{V}{\mu s}$. On the provided diagram, the slew rate is $\frac{10V}{20\mu s} = .5\frac{V}{\mu s}$.

4.2.2 Lab Results

Refer to Figure 1 for lab results. The rise time is roughly $38\mu s$ the overshoot is 25%. Also refer to Figure 2 for the slew rate, which is roughly 0.1 $\frac{V}{\mu s}$. The same circuit without the capacitor was tested in Figures 3 & 4.

4.3 Slew Rate Limiting

Refer to Figures 5 & 6.

4.4 Verification of Preliminary Question 2

4.4.1 Preliminary

With a 2kΩ output resistor in place, the maximum input voltage is 3.02 Volts. With a 100 Ω resistor in place, the maximum input voltage is 0.48 Volts. Refer to figure 7 for an expected plot of input to output.

4.4.2 Lab Results

Refer to Figures 8 & 9 for the lab results. They do not show the expected clipping.

4.5 Bandwidth

4.5.1 Preliminary

A gain of 40, 20, and 0 dB requires R_2 values of 100, 10, and 1 $k\Omega$, respecively. V_{in} was choosen to be 5V, which was too high and caused improper clipping.

4.5.2 Lab Results

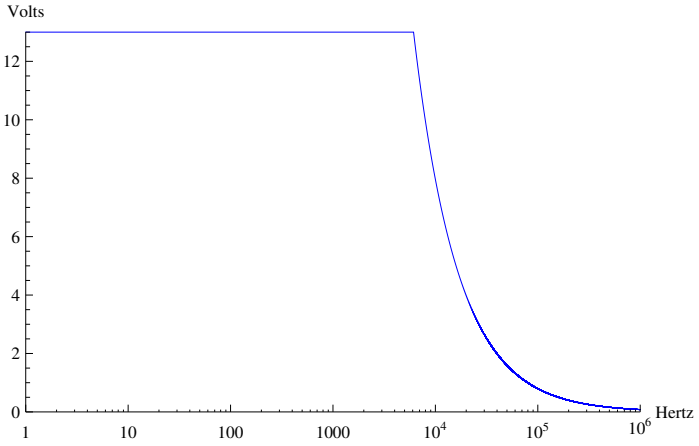
Refer to Figures 10 & 11.

5 Conclusions

The purpose of this lab was achieved. A number of circuits were built and their transfer functions measured and recorded. The measurements generally complied with the calculated values.

Appendix: Preliminary Questions

1



2

Refer to Section 4.4.

3

Full Power Bandwidth = 2652.58 Hz.

4

t_r is 1 $\frac{\mu s}{volt}$.

5

6

7

Refer to Section 4.2.

8

Refer to Section 4.1.

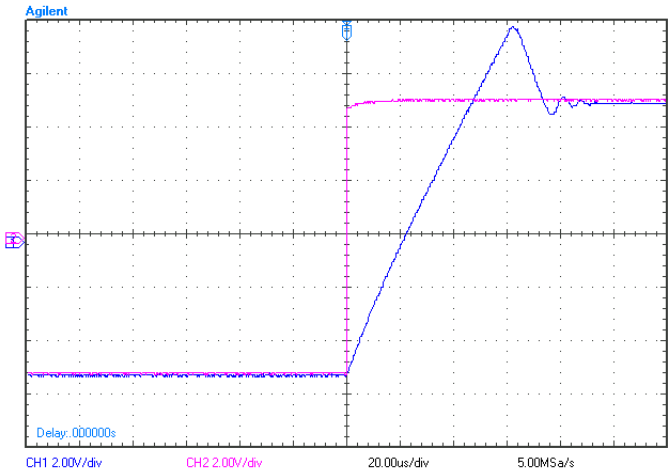


Figure 1: Lab Results for Figure 9

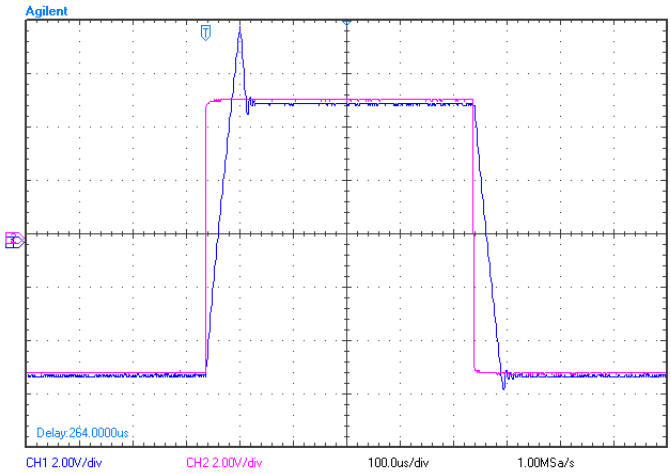


Figure 2: Lab Results for Figure 10

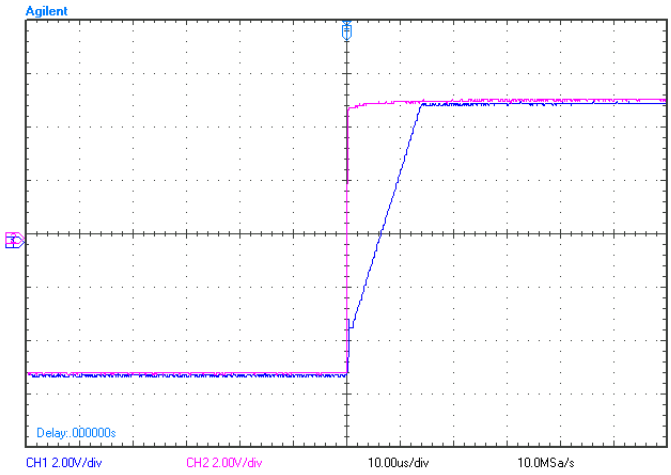


Figure 3: Lab Results for Figure 9

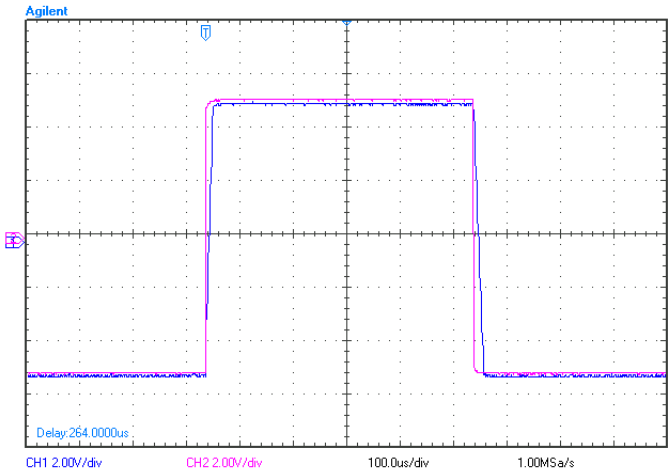


Figure 4: Lab Results for Figure 10

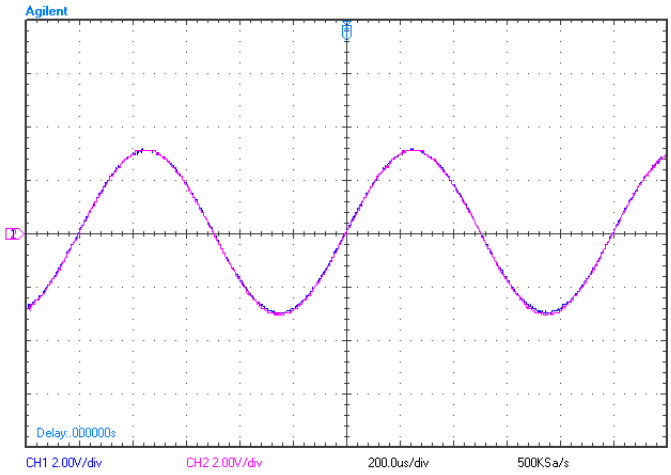


Figure 5: Lab Results for Procedure 3 — No Slewing

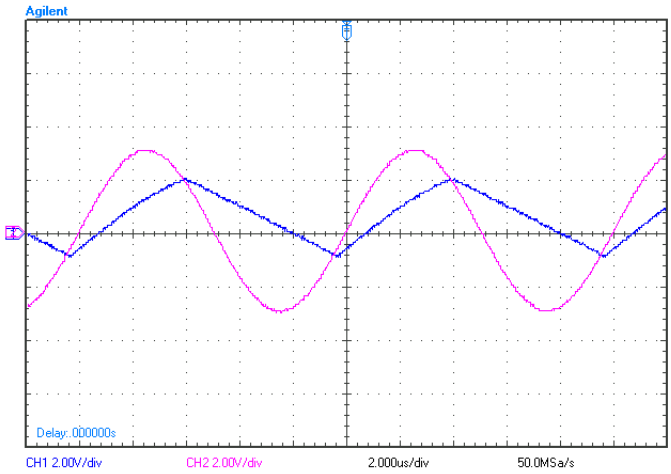


Figure 6: Lab Results for Procedure 3 — Slewing

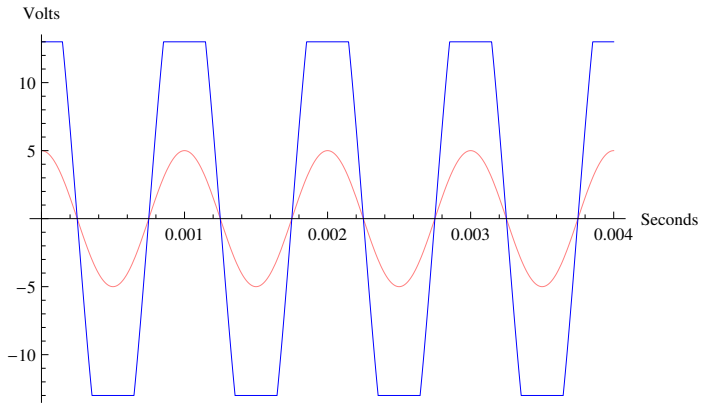


Figure 7: Preliminary Solution for Preliminary Question 3

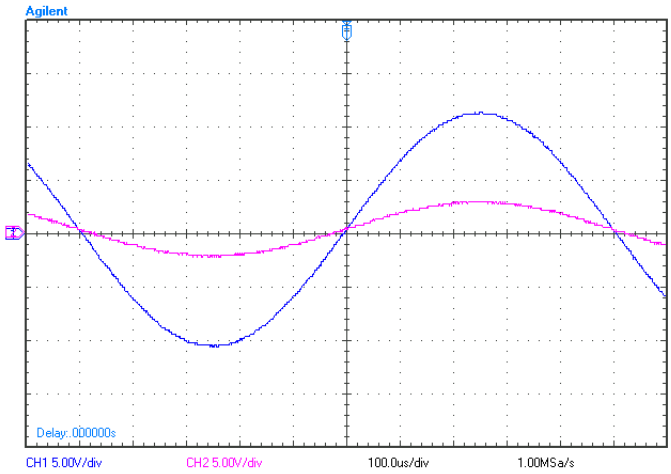


Figure 8: Lab Results for Preliminary Question 3 — $5V_{pp}$ input

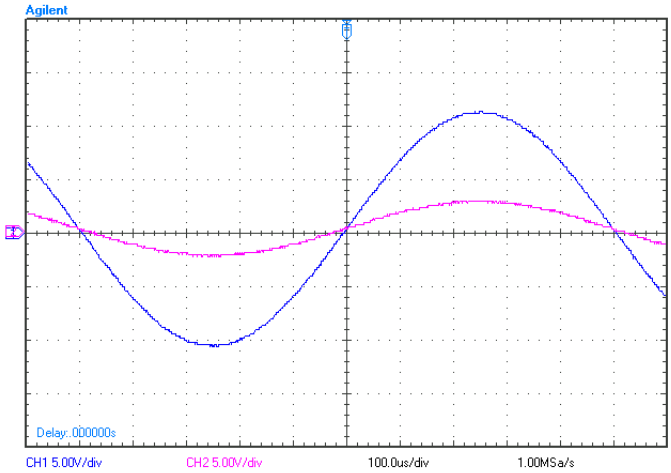


Figure 9: Lab Results for Preliminary Question 3 — $7V_{pp}$ input

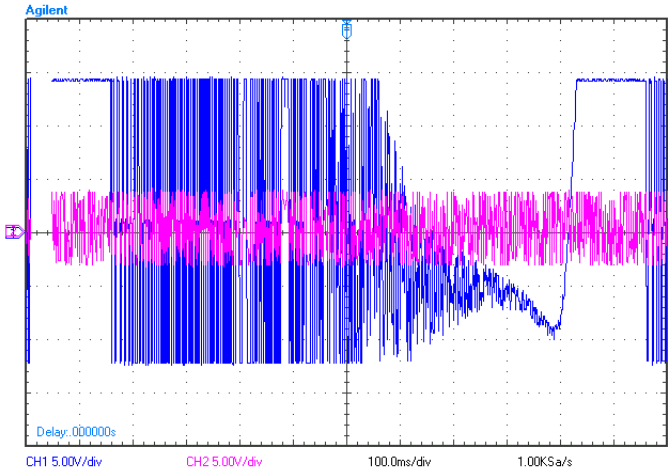


Figure 10: Lab Results for 40dB gain

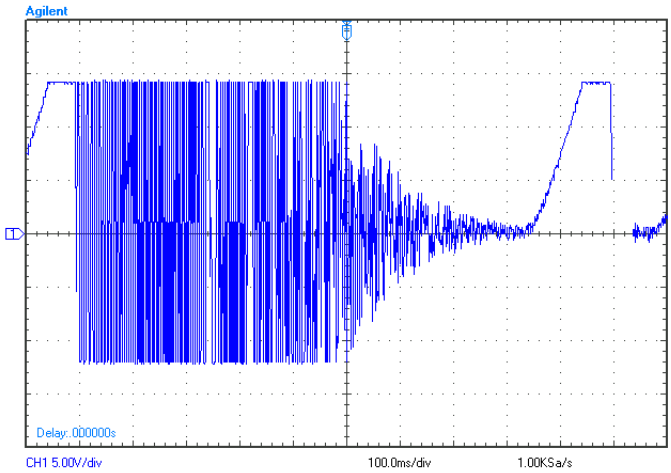


Figure 11: Lab Results for 20dB gain

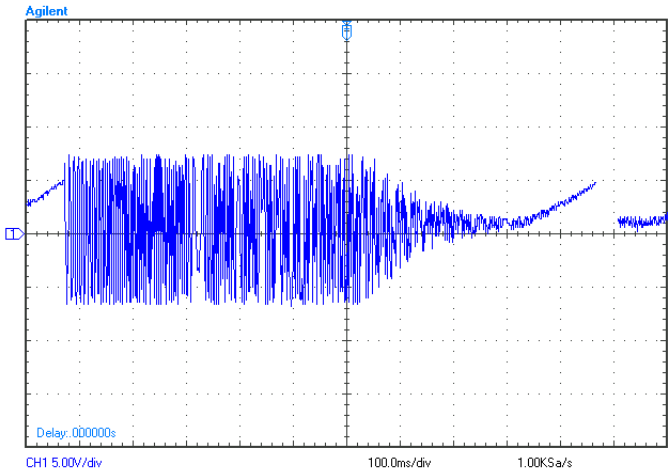


Figure 12: Lab Results for 0dB gain