Bus Cycle Count:	4								
Registers Changed									
PC	A1B2								
Bus Cycle Number	Address (Hex)	Data (Hex)	R / not(W)	not(UDS)	not(LDS)	AS	FC0	FC1	FC2
0	A1AC	11BC	1	0	0	0	0	1	1
1	A1AE	0065	1	0	0	0	0	1	1
2	A1B0	0004	1	0	0	0	0	1	1
3	A1E0	0065	0	0	1	0	1	0	1

Bus Cycle Count:	2								
Registers Changed									
PC	A1B2								
A4	A34D								
Bus Cycle Number	Address (Hex)	Data (Hex)	R / not(W)	not(UDS)	not(LDS)	AS	FC0	FC1	FC2
0	A1AC	49EB	1	0	0	0	0	1	1
1	A1AE	FF5F	1	0	0	0	0	1	1

Bus Cycle Count:	1								
Registers Changed									
PC	A1A0								
Bus Cycle Number	Address (Hex)	Data (Hex)	R / not(W)	not(UDS)	not(LDS)	AS	FC0	FC1	FC2
0	A1AC	60F2	1	0	0	0	0	1	1

List of signals for Supervisor Space
FC2, because it denotes supervisor space
not(A23) because that is always true in Supervisor space
not(AS) for sync

List of signals for User Data Space
FC0 because we want data space
not(FC2), because it we do not want supervisor space
A23 & A22 because those are always true in User Data space
not(AS) for sync

List of signals for User Program Space
not(FC0) because we want program space
not(FC2), because it we do not want supervisor space
A23 & not(A22) because those are always true in User Program space
not(AS) for sync

Exception Vector Table
The vector table resides entirely in the lowest addresses of the supervisor space.
All the vectors in that table except the ones associated with RESET reside in the supervisor data space.
RESET vectors reside in supervisor program space.