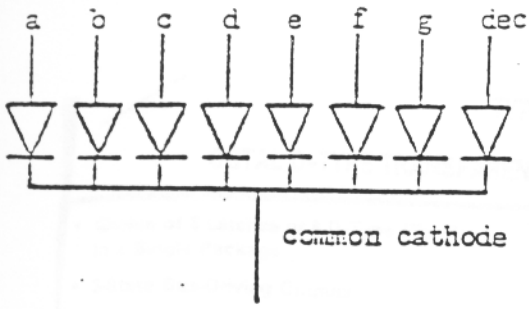
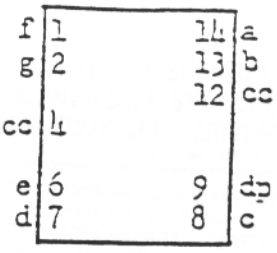
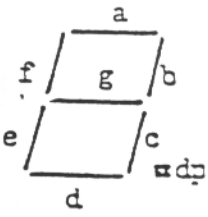






7448

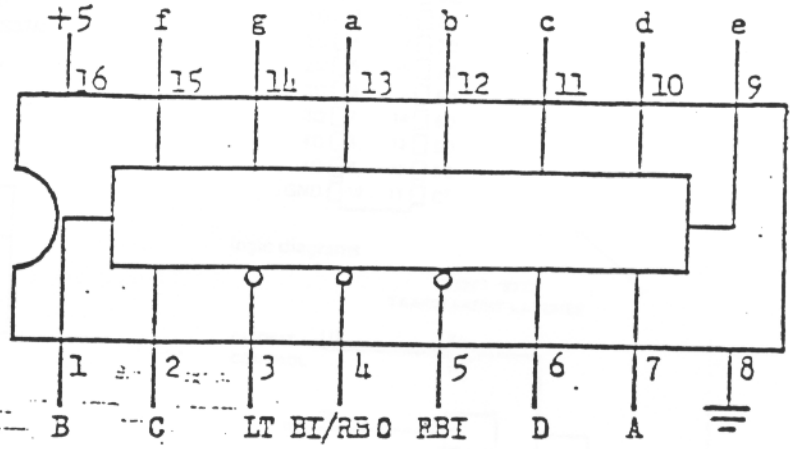
BCD/7-Segment Decoders/Drivers

BI Blanking Input

RBO Ripple Blanking Output

RBI Ripple Blanking Input

LT Lamp Test



NOTE: Any output can be directly connected to an LED since a dropping resistor is included in the output circuit.

Truth Table

HEXADECIMAL OR FUNCTION	INPUTS						BI/RBO	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H
A	H	X	H	L	H	L	H	L	L	L	H	H	L	H
B	H	X	H	L	H	H	H	L	L	H	H	L	L	H
C	H	X	H	H	L	L	H	L	H	L	L	L	H	H
D	H	X	H	H	L	H	H	H	L	L	H	L	H	H
E	H	X	H	H	H	L	H	L	L	L	H	H	H	H
F	H	X	H	H	H	H	H	L	L	L	L	L	L	L
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H

MOTOROLA

SN54/74LS373
SN54/74LS374

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

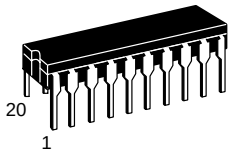
OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

LOW POWER SCHOTTKY

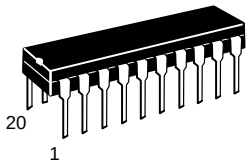
The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

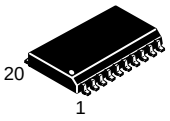
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0-O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

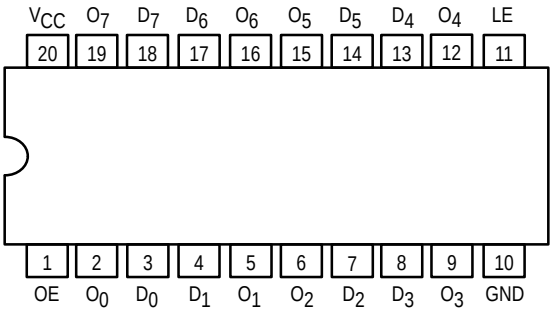
NOTES:
a) 1 TTL Units Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

ORDERING INFORMATION

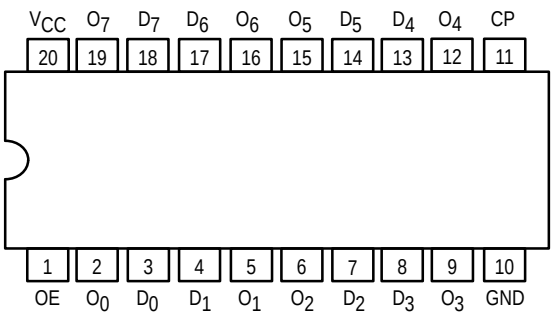
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

SN54/74LS373



SN54/74LS374



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

LS373

D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z*

LS374

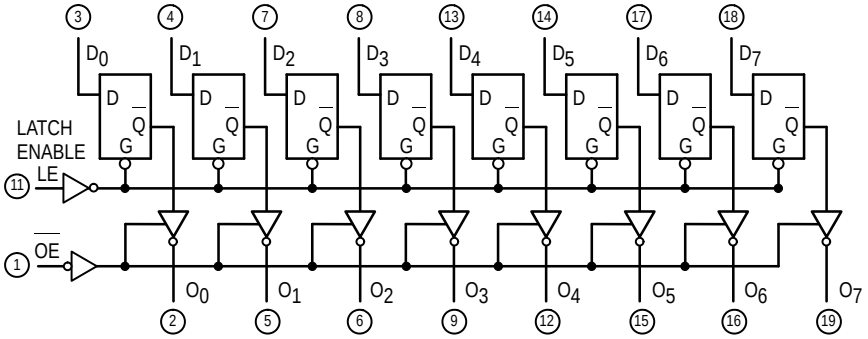
D_n	LE	$\overline{OE}$	O_n
H	↑	L	H
L	↑	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

* Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$).

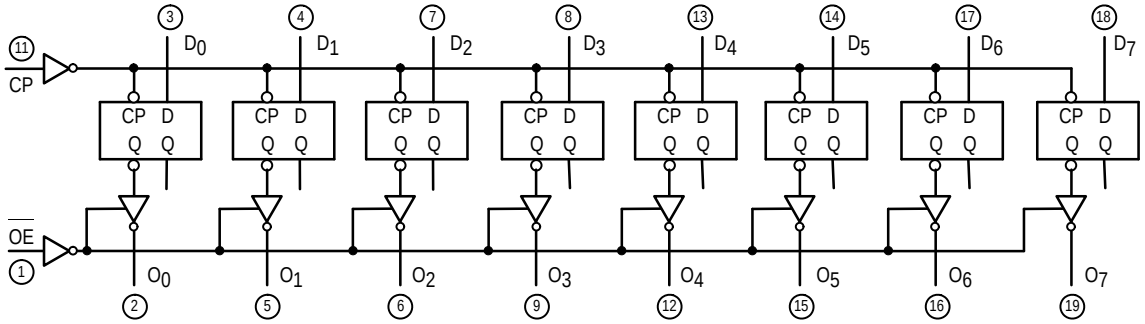
LOGIC DIAGRAMS

SN54LS/74LS373



V_{CC} = PIN 20
GND = PIN 10
◯ = PIN NUMBERS

SN54LS/74LS374



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				40	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits LS373 Min	LS373 Typ	LS373 Max	LS374 Min	LS374 Typ	LS374 Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency				35	50		MHz	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t_{PLH} t_{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits LS373 Min	LS373 Max	LS374 Min	LS374 Max	Unit
t_W	Clock Pulse Width	15		15		ns
t_s	Setup Time	5.0		20		ns
t_h	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

AC WAVEFORMS

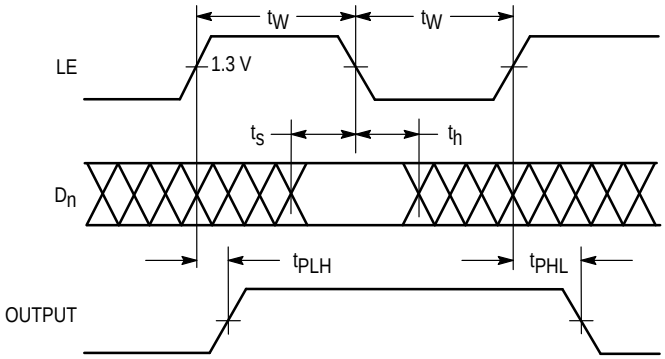


Figure 1

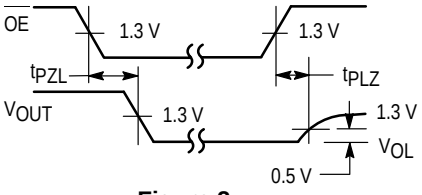


Figure 2

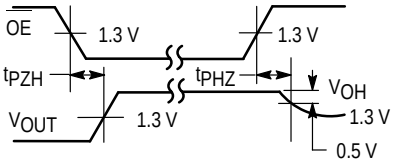
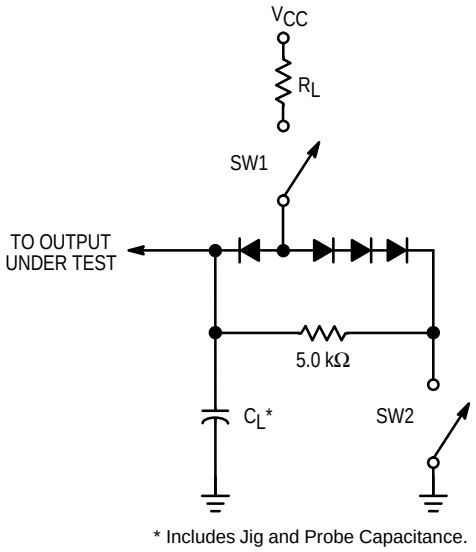


Figure 3

AC LOAD CIRCUIT



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 4

AC WAVEFORMS

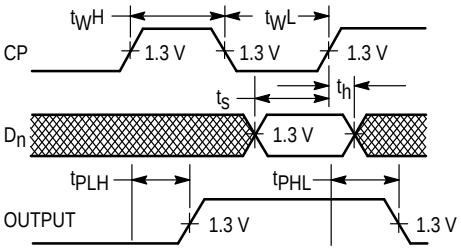


Figure 5

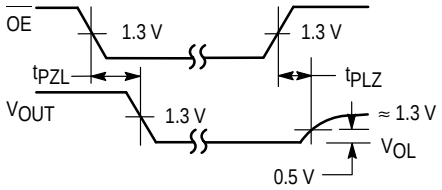


Figure 6

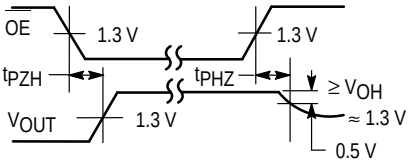
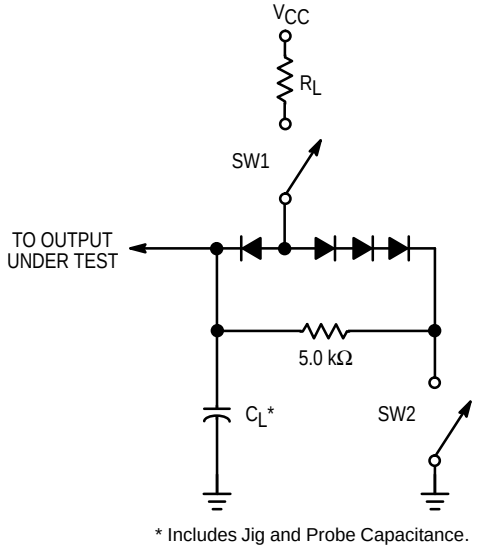


Figure 7

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 8

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed