4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

The MCM2114 series has a maximum current of 100 mA. Low power versions (i.e., MCM21L14 series) are available with a maximum current of only 70 mA.

- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Fully Static: Cycle Time = Access Time
- Maximum Access Time
  MCM2114-20/MCM21L14-20 200 ns
  MCM2114-25/MCM21L14-25 250 ns
  MCM2114-30/MCM21L14-30 300 ns
  MCM2114-45/MCM21L14-45 450 ns
- Fully TTL Compatible
- Common Data Input and Output
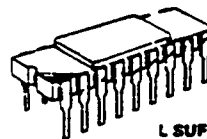- Three-State Outputs for OR-Ties
- Low Power Version Available

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

**P SUFFIX
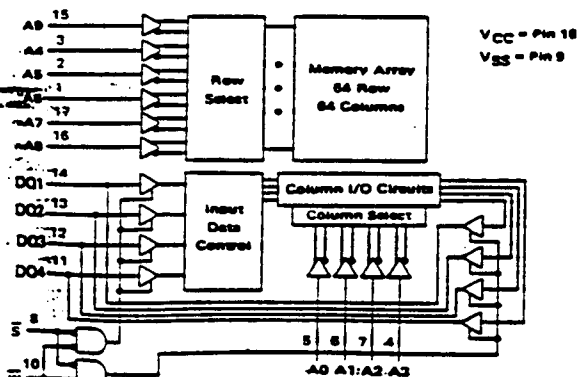PLASTIC PACKAGE
CASE 707**

**L SUFFIX
CERAMIC PACKAGE
CASE 680**

PIN ASSIGNMENT

A6	1	18	VCC
A5	2	17	A7
A4	3	16	A8
A3	4	15	A9
A0	5	14	DQ1
A1	6	13	DQ2
A2	7	12	DQ3
$\overline{S}$	8	11	DQ4
VSS	9	10	$\overline{W}$

PIN NAMES	
A0–A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ1–DQ4	Data Input/Output
VCC	Power (+5 V)
VSS	Ground

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	– 10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	–0.5 to +7.0	V
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	–65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	–0.5	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2114 Min	MCM2114 Typ	MCM2114 Max	MCM21L14 Min	MCM21L14 Typ	MCM21L14 Max	Unit
Input Load Current (All Input Pins, $V_{in} = 0$ to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
I/O Leakage Current (S = 2.4 V, $V_{DD} = 0.4$ V to VCC)	I_{LO}	–	–	10	–	–	10	μA
Power Supply Current ($V_{in} = 5.5$ V, $I_{DD} = 0$ mA, $T_A = 25°C$)	I_{CC1}	–	30	95	–	–	65	mA
Power Supply Current ($V_{in} = 5.5$ V, $I_{DD} = 0$ mA, $T_A = 0°C$)	I_{CC2}	–	–	100	–	–	70	mA
Output Low Current $V_{OL} = 0.4$ V	I_{OL}	2.1	6.0	–	2.1	6.0	–	mA
Output High Current $V_{OH} = 2.4$ V	I_{OH}	–	–1.4	–1.0	–	–1.4	–1.0	mA

NOTE: Duration not to exceed 30 seconds.

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	5.0	pF
Input/Output Capacitance ($V_{DD} = 0$ V)	$C_{I/O}$	5.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t / \Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels..0.8 Volt to 2.4 Volts   Input and Output Timing Levels..................................1.5 Volts
Input Rise and Fall Times...10 ns   Output Load..................................1 TTL Gate and $C_L = 100$ pF

READ (NOTE 1), WRITE (NOTE 2) CYCLES

| Parameter	Symbol	MCM2114-20 MCM21L14-20 Min	MCM2114-20 MCM21L14-20 Max	MCM2114-25 MCM21L14-25 Min	MCM2114-25 MCM21L14-25 Max	MCM2114-30 MCM21L14-30 Min	MCM2114-30 MCM21L14-30 Max	MCM2114-45 MCM21L14-45 Min	MCM2114-45 MCM21L14-45 Max	Unit
Address Valid to Address Don't Care	t_{AVAX}	200	–	250	–	300	–	450	–	ns
Address Valid to Output Valid	t_{AVQV}	–	200	–	250	–	300	–	450	ns
Chip Select Low to Data Valid	t_{SLQV}	–	70	–	85	–	100	–	120	ns
Chip Select Low to Output Don't Care	t_{SLQX}	20	–	20	–	20	–	20	–	ns
Chip Select High to Output High Z	t_{SHQZ}	–	60	–	70	–	80	–	100	ns
Address Don't Care to Output High Z	t_{AXQZ}	50	–	50	–	50	–	50	–	ns
Write Low to Write High	t_{WLWH}	120	–	135	–	150	–	200	–	ns
Write High to Address Don't Care	t_{WHAX}	0	–	0	–	0	–	0	–	ns
Write Low to Output High Z	t_{WLQZ}	–	60	–	70	–	80	–	100	ns
Data Valid to Write High	t_{DVWH}	120	–	135	–	150	–	200	–	ns
Write High to Data Don't	t_{WHDX}	0	–	0	–	0	–	0	–	ns

NOTES: 1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

MCM2114•MCM21L14

READ CYCLE TIMING (W̄ HELD HIGH)
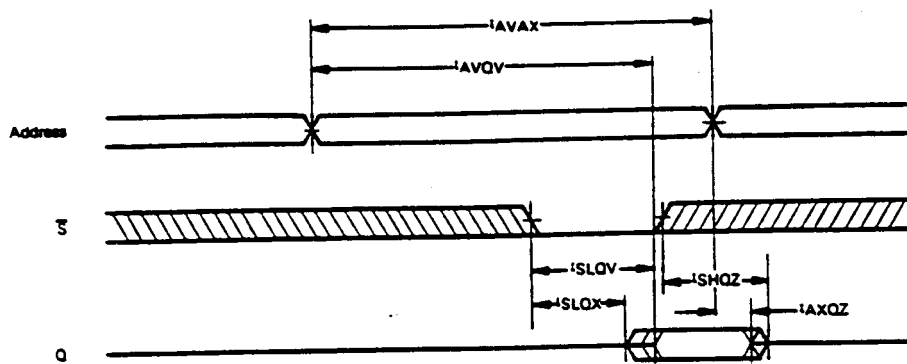
WRITE CYCLE TIMING (NOTE 3)
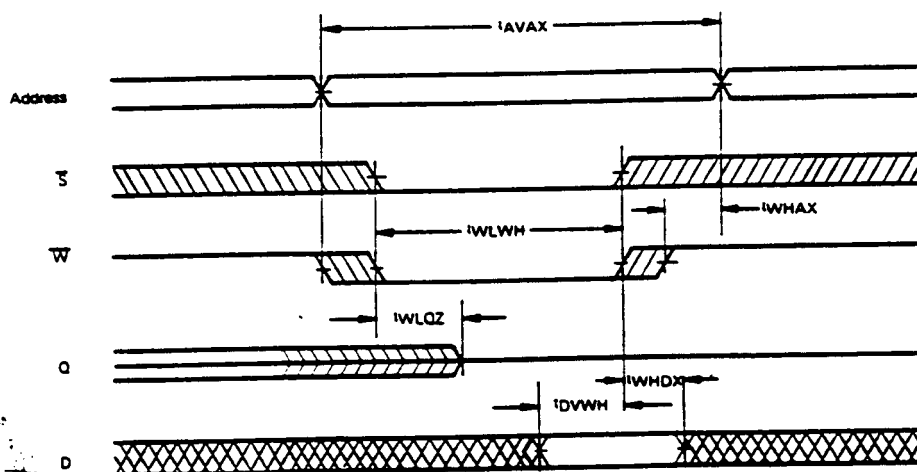
3. If the S̄ low transition occurs simultaneously with the W̄ low transition, the output buffers remain in a high-impedance state.

WAVEFORMS

Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE. ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	—	HIGH IMPEDANCE

SRAM