ECE441 Practice Questions II

1. What is meant by the terms partial address decoding and full address decoding?
2. What is a double bus fault?
3. Describe the importance of status and control registers in a programmable input/output device.
4. Carefully describe the order of the timing events involved in a synchronous read bus cycle.
5. A PIA must be initialized for the following conditions:

   PA0-PA2, PA6-PA7: Output
   PA3-PA5: Input
   PB0-PB6: Output
   PB7: Input

CA1 is active for positive transition and does not generate an interrupt.
CA2 is active for positive transition and is enabled to generate an interrupt.
CB1 is active for positive transition and is enabled to generate an interrupt.
CB2 is operating in pulse mode.
Determine the content of the following registers after reset and the above initialization:
DDRA $____ DDRB $_____ CRA $_____ CRB $_____

6. Design a memory and input/output board consisting of the following components:
   ROM $10000 - $1FFFF, Use 32K x 8 ROM Chips
   Output Port, One Byte, Location $20000, Use 74373 Chip
   One PIA, to be accessed using D0-D7 data lines of the microprocessor, with a starting address at $20001, Assume the interrupt level 7 is used for both the IRQA* and IRQB* lines.

   a) You must show the address map below for your design.

	A23 … A20	A19 … A16	A15…A12	A11…A3A2A1	UDS*	LDS*
ROM1						
ROM2						
OUTPUT						
PIA						
OTHERS						

   b) Find (include value 0 or 1) and list the required signals (control, minimum number of address lines, etc.) for decoding and selecting ROM,. Output port and PIA. Note that there are other devices using memory in the range of $000000 - $00FFFF.

   c) Show your hardware design for accessing ROM, Output Port and PIA. Assume ROM is faster than the microprocessor and no delay data acknowledge is required. Mark all required signals and use any TTL logic that you think is suitable for your design.

7. How many bytes will the following program move from one region of memory to another region of memory? Explain your answer. Note: Register A1 = $A100 and A0 = $A000. ORG is $1000 (Be careful answering this question).

```
      ORG $1000
      MOVE.W #$1000, D0
REP   MOVE.W 0(A0, D0), 0(A1, D0)
      DBRA D0, REP
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