Determine the number of bus cycles, the value of the function control lines, the address bug, the data bus, $R/\overline{W}$, $\overline{UDS}$, $\overline{LDS}$ and the $\overline{AS}$ in each bus cycle while executing the following instructions. If you think any of the requested information is unknown due to inadequate information, write unknown in the table.

Note: Assume each of these instructions are executing at location $A000 when the SR=$2700, D0=$D0, D1=$D1, D2=$D2, D3=$D3, D4=$D4, D5=$D5, D6=$D6, D7=$D7, A0=$A000, A1=$A100, A2=$A200, A3=$A300, A4=$A400, A5=$A500, A6=$A600, A7=$A700.

Ignore pre-fetch operation of the microprocessor.

MOVE.L $7000, $B100 Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									
6									
7									
8									

LEA +5(A3), A2 Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									

MOVE.L (A1), (A2) Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									
6									
7									
8									

CLR.L **$A000** Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									
6									
7									
8									

ROR **(A2)+** Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									

PEA **-15(A2)** Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									

ADDI.L **#$2, 2(A2,A0)** Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									
6									
7									
8									

BRA **$3000** Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									
6									
7									
8									

MOVEM.L **(A3)+, A0/D0** Number of Bus Cycles : _____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1									
2									
3									
4									
5									
6									
7									
8									

Solutions

MOVE.L $7000, $B100 Number of Bus Cycles : _____8_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	23F8	1	0	0	0	1	1	0
2	A002	7000	1	0	0	0	1	1	0
3	A004	0000	1	0	0	0	1	1	0
4	A006	B100	1	0	0	0	1	1	0
5	7000	U	1	0	0	0	1	0	1
6	7002	U	1	0	0	0	1	0	1
7	B100	U	0	0	0	0	1	0	1
8	B102	U	0	0	0	0	1	0	1

LEA +5(A3), A2 Number of Bus Cycles : _____2_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	45EB	1	0	0	0	1	1	0
2	A002	0005	1	0	0	0	1	1	0
3									
4									

MOVE.L (A1), (A2) Number of Bus Cycles : _____5_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	2491	1	0	0	0	1	1	0
2	A100	U	1	0	0	0	1	0	1
3	A102	U	1	0	0	0	1	0	1
4	A200	U	0	0	0	0	1	0	1
5	A202	U	0	0	0	0	1	0	1
6									
7									
8									

CLR.L **$A000** Number of Bus Cycles : _____7_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	42B9	1	0	0	0	1	1	0
2	A002	0000	1	0	0	0	1	1	0
3	A004	A000	1	0	0	0	1	1	0
4	A000	42B9	1	0	0	0	1	0	1
5	A002	0000	1	0	0	0	1	0	1
6	A002	0000	0	0	0	0	1	0	1
7	A000	0000	0	0	0	0	1	0	1
8									

ROR **(A2)+** Number of Bus Cycles : _____3_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	E6DA	1	0	0	0	1	1	0
2	A200	U	1	0	0	0	1	0	1
3	A200	U	0	0	0	0	1	0	1
4									
5									

PEA **-15(A2)** Number of Bus Cycles : _____4_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	486A	1	0	0	0	1	1	0
2	A002	FFF1	1	0	0	0	1	1	0
3	A6FE	A1F1	0	0	0	0	1	0	1
4	A6FC	0000	0	0	0	0	1	0	1
5									

ADDI.L **#$2, 2(A2,A0)** Number of Bus Cycles : _____8_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	06B2	1	0	0	0	1	1	0
2	A002	0000	1	0	0	0	1	1	0
3	A004	0002	1	0	0	0	1	1	0
4	A006	8002	1	0	0	0	1	1	0
5	4202	U	1	0	0	0	1	0	1
6	4204	U	1	0	0	0	1	0	1
7	4204	U	0	0	0	0	1	0	1
8	4202	U	0	0	0	0	1	0	1

BRA **$3000** Number of Bus Cycles : _____2_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	6000	1	0	0	0	1	1	0
2	A002	8FFE	1	0	0	0	1	1	0
3									
4									
5									
6									
7									
8									

MOVEM.L **(A3)+, A0/D0** Number of Bus Cycles : _____6_____

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	FC2	FC1	FC0
1	A000	4CDB	1	0	0	0	1	1	0
2	A002	0101	1	0	0	0	1	1	0
3	A300	U	1	0	0	0	1	0	1
4	A302	U	1	0	0	0	1	0	1
5	A304	U	1	0	0	0	1	0	1
6	A306	U	1	0	0	0	1	0	1
7									
8									