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ECE 446 – EXAM 1

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Exam is closed book and closed notes. YOU MUST SHOW ALL YOUR WORK

Problem 1. (12 points)

a) Describe the Schmitt-trigger input. What is the meaning of the hysteresis?

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Schmitt triggers lock to the rails after a trigger voltage, and only transition after the input transitions passes an opposing trigger voltage. This dependency on past states is the hysteresis

b) Describe the three-state buffer. What is the floating state?

three state buffers allow a gate to be high or low, or also be a gate to be driven state driving neither high nor low, so High-Z busses can be shared

c) Draw the CMOS three-state buffer circuit diagram for the logic symbol below:

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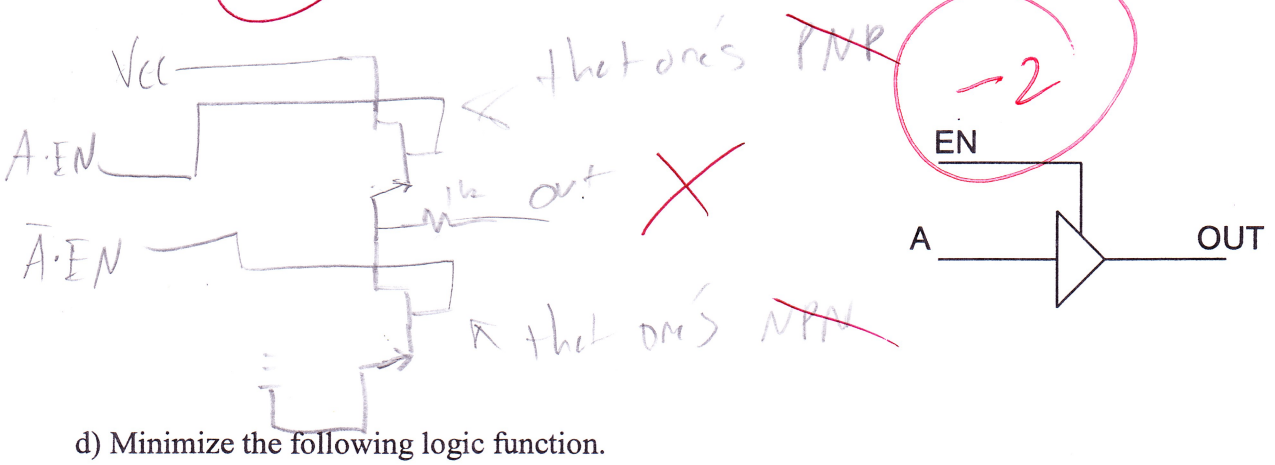
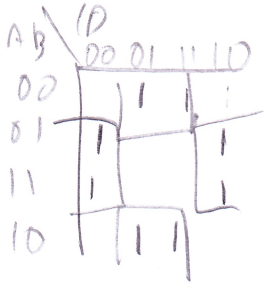


d) Minimize the following logic function.

$\Sigma ABCD\ (1, 3, 4, 6, 9, 11, 12, 14)$



$\bar{D}B + \bar{C}B$

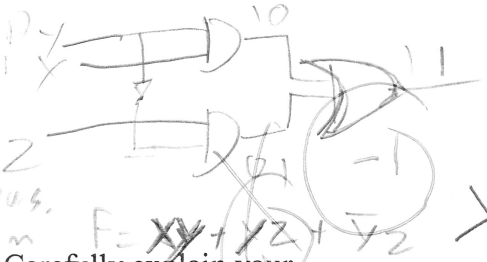
-1

Problem 2. **(12 points)**

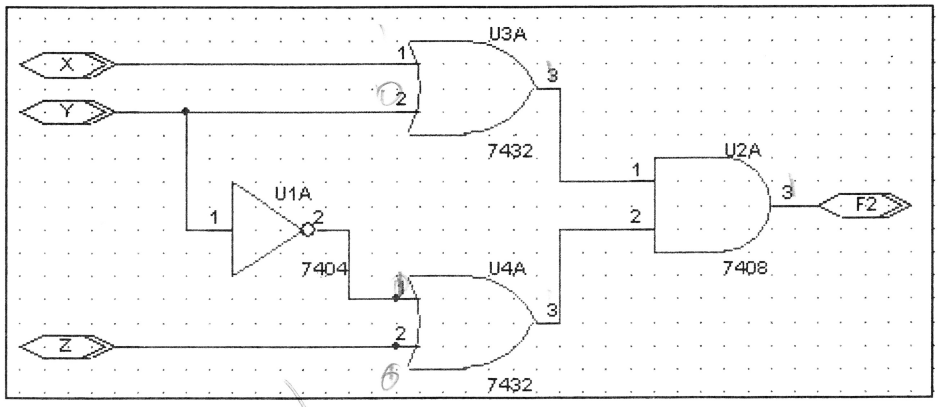
a) Describe Static 0-Hazard and Static 1-Hazard.

b) Determine whether the logic expression for F_1 contains static hazard. Carefully explain your answer. Redesign this expression to remove the hazard if required.

$$F_1 = XY + \bar{Y}Z$$

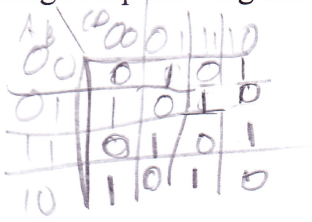


c) Determine whether the logic expression for F_2 contains a static hazard. Carefully explain your answer. Redesign this expression to remove the hazard if required.



Problem 3. **(8 points)**

(a) Draw the Karnaugh Map showing the minterms for a four-bit even parity function.



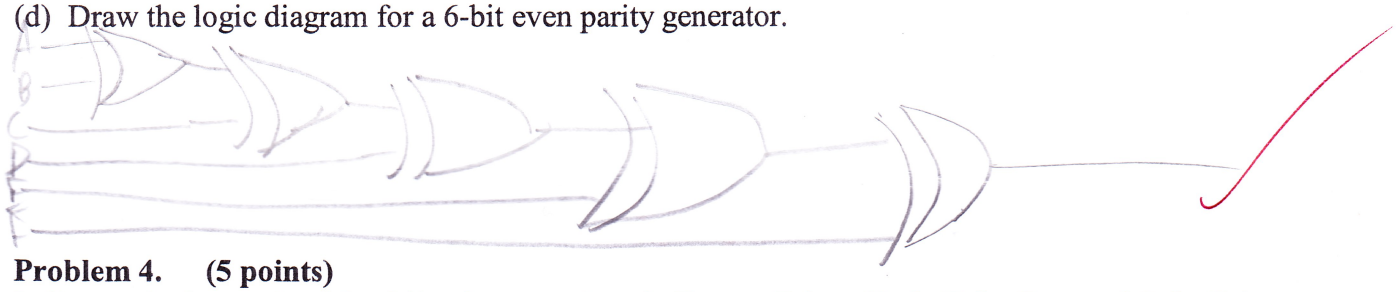
(b) In general how many minterms does an n-input parity function have? Explain your answer.

2^{n-1}, half of the permutations

(c) In general, how many product terms does an n-input even parity function have after minimization? Explain your answer.

2^{n-1}, they don't minimize

(d) Draw the logic diagram for a 6-bit even parity generator.



Problem 4. **(5 points)**

Indicate whether each of the following equations is True or False. Circle T for True and F for False.

a) W.X+Y'+Z=(W+Y'+Z).(X+Y'+W'.Z+W.Z) T or F

b) (W.X'.Y.Z+W.X.Y.Z')'= (W'+X+Y'+Z').(W'+X'+Y'+Z) T or F

c) ΣWXYZ(2,7,9,13) = W'.X'.Y.Z'+W'X.Y.Z+W'.X'.Y'.Z+W.X.Y'.Z T or F

but you probably meant to have W'XYZ, in which case true

d) W $\oplus$ X $\oplus$ Y $\oplus$ Z= ΣWXYZ(1,2,4,7,8,11,13,15) T or F

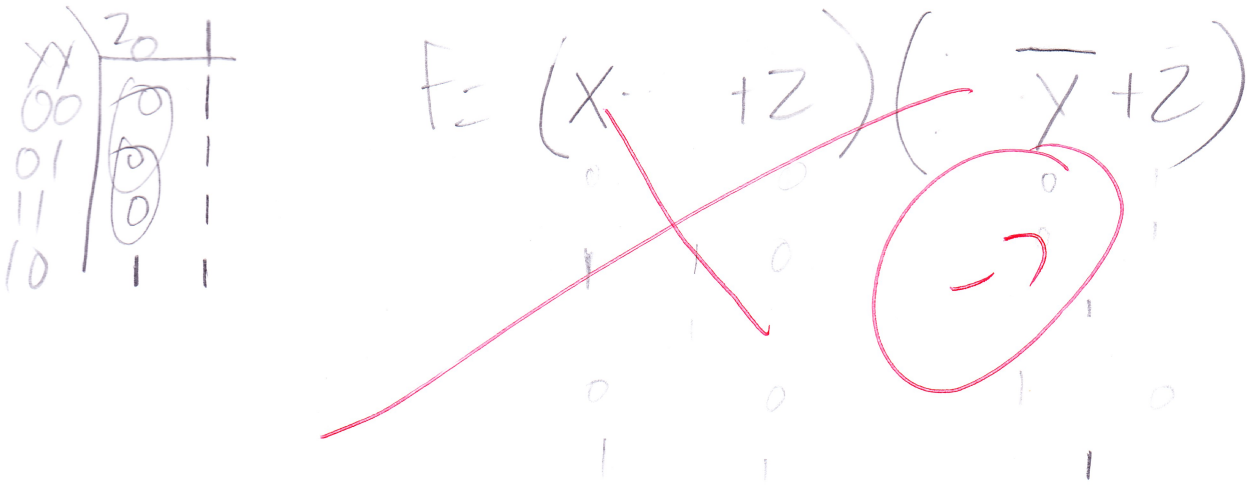
-2

e) Because of Duality Law $Y'Z' = (Y + Z)'$ T or F

Problem 5. (15 points)

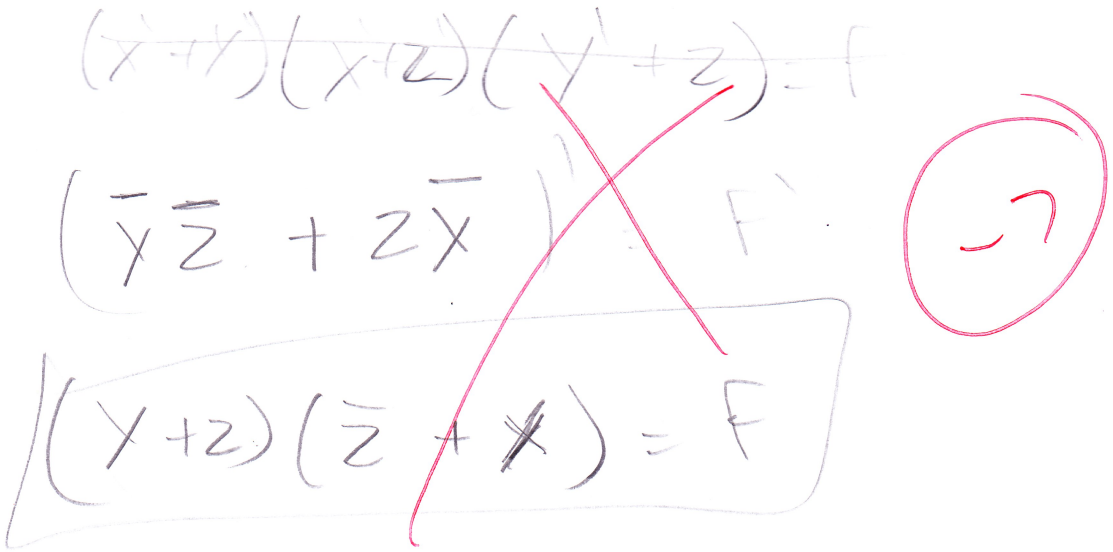
a) Use properties of switching algebra to convert the following function to the product of the sums (POS) expression.

$F = Z+X\,Y'\,Z'$ where X, Y, and Z are input variables.



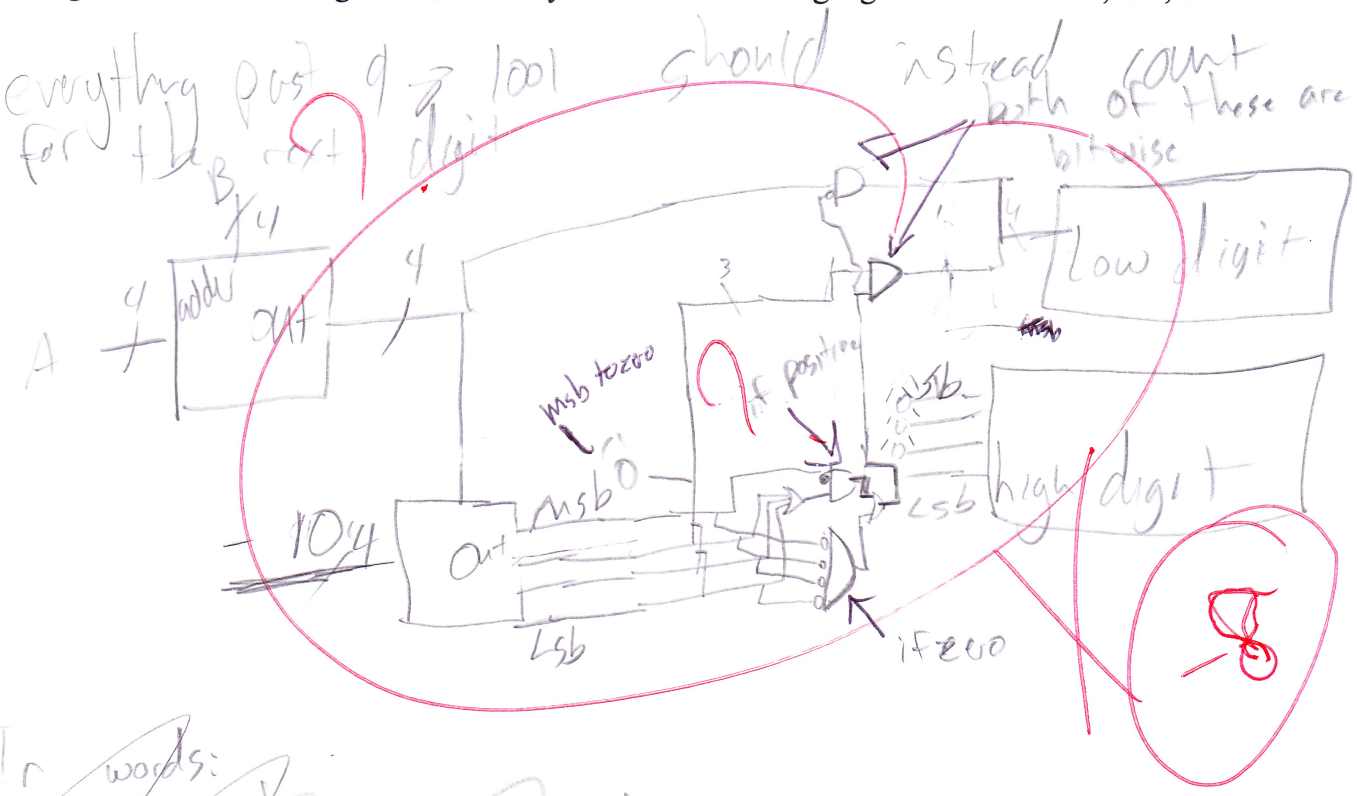
b) Convert the Boolean function below to maxterm canonical form using De Morgan's laws.

$F = (X\,Y + X\,Z + YZ')$ where X, Y, and Z are input variables.



Problem 6. **(12 points)**

Design a BCD adder using two 4-bit binary adders and other logic gates such as AND, OR, and NOT.



In words:

add the two num bus (which must be 0-9)

Subtract 10 from the result.

if the result of the subtraction is ≥ 0

then → $(b_3(b_2 \text{ or } b_1)b_0) + (b_3 b_2 b_1 b_0)$ b_3 = msb b_0 = lsb

and set the high digit to 1

and set the bottom three bits of the low digit

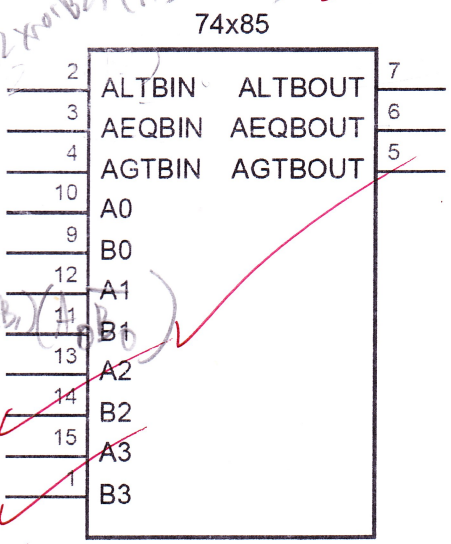
to the bottom three bits of the subtraction outcome

by anding each with that expression.

and the first adders outcome with

Problem 7. (16 points)

a) Write the logic expressions for 74x85, the 4-bit comparator: A=B, A>B, A<B, ALTBOUT, AEQBOUT, and AGTBOUT.



$A=B = (A0 \text{ xnor } B0)(A1 \text{ xnor } B1)(A2 \text{ xnor } B2)(A3 \text{ xnor } B3)$

$A>B = A_3\overline{B_3} + (A_3 \text{ xnor } B_3)A_2\overline{B_2} + (A_3 \text{ xnor } B_3)(A_2 \text{ xnor } B_2)(A_1\overline{B_1}) + (A_3 \text{ xnor } B_3)(A_2 \text{ xnor } B_2)(A_1 \text{ xnor } B_1)(A_0\overline{B_0})$

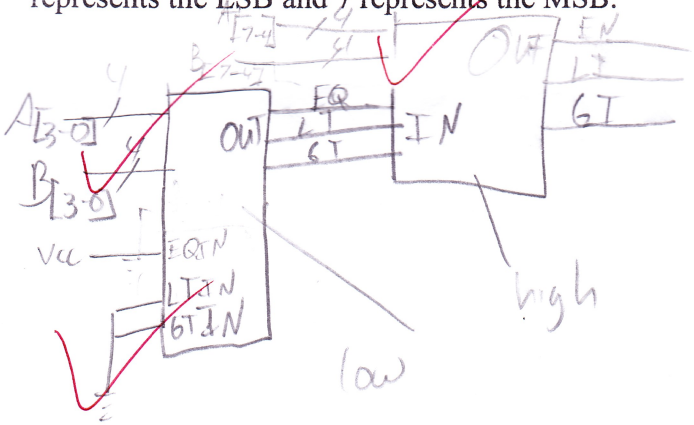
$A<B = \overline{(A=B)}\,\overline{(A>B)}$

$AGTBOUT = A>B + (A=B)(AGTBIN)$

$ALTBOUT = A<B + (A=B)(ALTBIN)$

$AEQBOUT = (AEQBIN)\cdot(A=B)$

b) Use two 74x85 chips and design an 8-bit comparator to compare X0-X7 with Y0-Y7 where 0 represents the LSB and 7 represents the MSB.



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c) Use the output of the 8-bit comparator and write the expressions for

(X0-X7) NE (Y0-Y7) ---- (X not equal Y)

(X0-X7) GE (Y0-Y7) ---- (X greater than or equal Y)

(X0-X7) LE (Y0-Y7) ---- (X less than or equal Y)

$AEQBOUT_{high}$

$AEQBOUT_{high} + AGTBOUT_{high}$

$AEQBOUT_{high} + ALTBOUT_{high}$

Problem 8. **(10 points)**

a) Carefully describe the design of error correction Hamming code for a 16-bit data word.

by putting parity bits at bit locations corresponding to a power of 2 (1, 2, 4, 8, 16) and setting each parity bit to the xor of a number of the data bits, you can ensure data integrity (by having parity bits on the receiver) and if integrity is not maintained in transit, the parity bits will correspond to the incorrect bit, which can be noted and corrected.

21 BITS

b) Describe the method of detecting and correcting a one bit error in a 16-bit data word using the Hamming code.

After receiving a hamming code encoded signal, if any of the parity bits are nonzero, an error occured in transit. If that is the case, the parity bits will read out the bit position at which the error occured. This bit can be flipped and the single bit error corrected.

Write expressions X -5